

56F8006

Preliminary Chip Errata

56F8006 Digital Signal Controller

This document reports errata information on chip revision A. Errata numbers are in the form n.m, where n is the number of the errata item and m identifies the document revision number. This document is a pre-publication draft.

Chip Revision A Errata Information:

The following errata items apply only to Revision A 56F8006 devices. These parts are marked with 1M53M.

Errata Number	Description	Impact and Workaround
1.0	If the Watch Dog Timer (WDT) is used to wake the device from the Partial Power Down (PPD) mode, the WDT may count down too quickly.	Impact: The device may not wake from the PPD mode reliably. Workaround: Use the RTC timer to wake from the PPD mode to the Run mode, rather than the WDT or use a timeout longer than 100MS for the Watch Dog Timer to wake the device from Partial Power Down mode.
2.0	The internal relaxation oscillator does not meet the specifications for frequency.	Impact: Peripherals may operate with unexpected timing. Workaround: If stricter timing is required, use an external crystal, resonator, or oscillator module of the required frequency specification.
3.0	The ADC Conversion Complete interrupt is asserted and then removed if sample_select ping-pongs to other ADC register-set prior to the CPU servicing the interrupt request.	Impact: The ADC interrupt signal may not interrupt the core. Workaround: Make the ADC a higher priority interrupt or poll the ADC in a timer or PWM interrupt handler rather than use the ADC interrupts.
4.0	A hardware trigger generated through a PGA to an ADC may upset the use of Software triggers with the PGA.	Impact: Incorrect triggering of the ADC by the PGA may result in wrong data from the ADC. Workaround: Avoid the use of the software trigger mode of the PGA.

Errata Sheet History

Previously Documented in Past Errata Sheets	Correction

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Europe, Middle East, and Africa:

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Technical Information Center
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+46 8 52200080 (English)
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Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
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support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
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