



BY BONNIE BAKER



Understanding FFT plots

You can generate an FFT (fast-Fourier-transform) plot by periodically collecting a large number of conversion samples from the output of an ADC. Typically, ADC manufacturers use a single-tone, full-scale analog input signal for the performance curves in product data sheets. You take data from these conversions and create a plot similar to the one in **Figure 1**. The frequency scale of this plot is always linear, from zero to the converter's sampling frequency divided by two.

You generate the plot by applying a sampling frequency of 100k samples/sec to a 12-bit ADC with an analog input signal of 9.9 kHz. The signal at 9.9 kHz is the fundamental input signal (A). The fundamental input-signal spur reaches almost 0 dB.

The specifications of interest in an FFT plot are the fundamental input signal, the SNR (signal-to-noise ratio), the THD (total harmonic distortion), and the average noise floor. A useful way of determining noise in an ADC

circuit is with the SNR (B), the ratio of signal power to noise power. The SNR of the FFT calculation is a combination of several noise sources, including the quantization error of the ADC, the internal noise of the ADC, noise from the voltage reference, and noise from the driving amplifier. The theoretical limit of SNR is $6.02n + 1.76$ dB, where n is the number of converter bits.

The THD (C) quantifies the amount of distortion in the system.

The THD is the ratio of the root-mean-square sum of the powers of the harmonic components, or spurs, to the input-signal power. Spurs resulting from the non-linearity of the ADC appear as whole-number multiples of the input signal's frequency, or fundamental frequency. Most manufacturers use the first seven to nine harmonic components in their THD calculations.

If the ADC creates spurs, it most likely

has some INL (integral nonlinearity) errors. Spurs can also come from the input signal through the signal source or the driving amplifier. If the driving amplifier is the culprit, it may have crossover distortion, be unable to drive the ADC, or be bandwidth-limited. Injected noise from other places in the circuit, such as digital clock sources or the mains frequency, can also create spurs in the FFT result.

In an FFT representation of converter data, the average noise floor (D) is a root-mean-square combination of all the bins within the FFT plot but excludes the input signal and signal harmonics. You should choose the number of samples versus the number of ADC bits so that the noise floor is below any spurs of interest. With these considerations in mind, the theoretical average FFT noise floor is $6.02n + 1.76 + 10 \log[(3 \times M) / (\pi \times \text{ENBW})]$, where M is the number of data points in the FFT, ENBW is the equivalent noise bandwidth of the window function, and n is the number of bits of the ADC. A reasonable number of samples for the FFT of a 12-bit converter is 4096. **EDN**

REFERENCES

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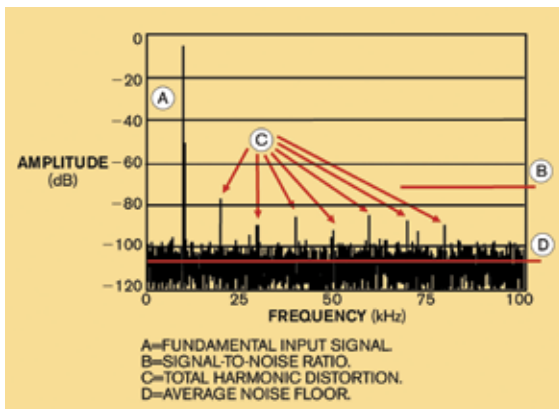


Figure 1 There are 4096 data samples from a 12-bit converter in this FFT plot. The frequency spectrum for a 4096-point FFT is 100 kHz with $f_{IN} = 9.9$ kHz.

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